CLAIMS

What is claimed is:

1. An information handling system having power supply shutdown control, said system comprising:

an information handling system having a power supply, the power supply adapted for receiving power from an external power source and providing voltages necessary to power the information handling system, the power supply having an on-input and an inhibit-input, wherein the on-input is used to turn the power supply on and off and the inhibit-input prevents the power supply from being turned on when at a first logic level and allows the power supply to be turned on when at a second logic level; and

a shutdown control circuit monitoring at least one voltage from the power supply, the shutdown control circuit having an output coupled to the inhibit-input of the power supply, wherein when the at least one voltage is less than a first voltage value the shutdown control circuit output is set to the first logic level, and when the at least one voltage is less than a second voltage value the shutdown control circuit output is reset to the second logic level.

2. The information handling system according to claim 1, wherein the on-input is coupled to an on-off power switch.

3. The information handling system according to claim 1, wherein the on-input is coupled to a power pushbutton and a control circuit.

4. The information handling system according to claim 1, wherein the shutdown control circuit comprises:

a voltage reset monitor having an output and an input coupled to the at least one voltage from the power supply, wherein the voltage reset monitor output is at a first logic level when the at least one voltage is greater than or equal to the first voltage value and at a second logic level when the at least one voltage is less than the first voltage value;

a voltage detector having an input coupled to the at least one voltage from the power supply and an output, wherein the voltage detector output is at the first logic level when the at least one voltage from the power supply is greater than or equal to the second voltage value and is at the second logic level when the at least one voltage is less than the second voltage value;

a memory circuit having an input coupled to the output of the voltage reset monitor, clear input coupled to output of the voltage detector, and an output coupled to the inhibit-input of the power supply; and

a continuous power source that supplies power to the voltage detector and the memory circuit; wherein when the voltage reset monitor output goes from the first logic level to the second logic level the memory circuit output is set to the first logic level and when the voltage detector output is at the second logic level the memory circuit output is reset to the second logic level.

5. The information handling system according to claim 4, wherein the voltage detector is a transistor biased to cutoff when its input is less than the second voltage value.

6. The information handling system according to claim 5, wherein the transistor is a field effect transistor (FET).

7. The information handling system according to claim 6, wherein the FET is an enhancement mode FET.

8. The information handling system according to claim 4, wherein the memory circuit is a D flip-flop, wherein the voltage reset monitor output is coupled to a D-input of the D flip-flop, the voltage detector output is coupled to a clear input of the D flip-flop, and a Q-output of the D flip-flop is coupled to the inhibit-input of the power supply.

9. The information handling system according to claim 4, wherein the continuous power source is a battery.

10. A method for preventing a power supply from being re-energized before at least one voltage therefrom is below a minimum voltage level, said method comprising the steps of:

providing a power supply in an information handling system that receives power from an external power source and provides voltages necessary to power the information handling system, the power supply having an on-input and an inhibit-input, wherein the on-input turns the power supply on and off and the inhibit-input prevents the power supply from being turned on when at a first logic level and allows the power supply to be turned on when at a second logic level; and

monitoring at least one voltage from and controlling the power supply with a shutdown control circuit, the shutdown control circuit having an output coupled to the inhibit-input of the power supply, wherein when the at least one voltage is less than a first voltage value the shutdown control circuit prevents the power supply from being turned on until the at least one voltage is less than a second voltage value.

11. The method according to claim 10, further comprising the steps of turning the power supply on and off with a switch.

12. The method according to claim 11, wherein the switch is a momentary pushbutton.

13. The method according to claim 12, wherein the momentary pushbutton is coupled to the power supply with an on-off control circuit.

14. The method according to claim 10, wherein the steps of monitoring at least one voltage from and controlling the power supply, comprise the steps of:

providing a voltage reset monitor for monitoring the at least one voltage from the power supply, wherein the voltage reset monitor is at a first logic level when the at least one voltage is greater than or equal to the first voltage value and at a second logic level when the at least one voltage is less than the first voltage value;

providing a voltage detector for monitoring the at least one voltage from the power supply, wherein the voltage detector is at the first logic level when the at least one voltage from the power supply is greater than or equal to the second voltage value and is at the second logic level when the at least one voltage is less than the second voltage value;

providing a memory circuit coupled to the voltage reset monitor, the voltage detector and to the inhibit-input of the power supply; and

providing a continuous power source for supplying power to the voltage detector and the memory circuit; wherein when the voltage reset monitor goes from the first logic level to the second logic level the memory circuit is set to the first logic level and when

the voltage detector is at the second logic level the memory circuit is reset to the second logic level.

15. A apparatus for preventing a power supply from being re-energized before at least one voltage therefrom is below a minimum voltage level, said apparatus comprising:

a voltage reset monitor having an output and an input coupled to at least one voltage from a power supply, wherein the voltage reset monitor output is at a first logic level when the at least one voltage is greater than or equal to a first voltage value and at a second logic level when the at least one voltage is less than the first voltage value;

a voltage detector having an input coupled to the at least one voltage from the power supply and an output, wherein the voltage detector output is at the first logic level when the at least one voltage from the power supply is greater than or equal to the second voltage value and is at the second logic level when the at least one voltage is less than the second voltage value;

a memory circuit having an input coupled to the output of the voltage reset monitor, clear input coupled to output of the voltage detector, and an output coupled to the inhibit-input of the power supply; and

a continuous power source that supplies power to the voltage detector and the memory circuit; wherein when the voltage reset monitor output goes from the first logic level to the second logic level the memory circuit output is set to the first logic level and when the voltage detector output is at the second logic level the memory circuit output is reset to the second logic level.

16. The apparatus according to claim 15, wherein the voltage detector is a transistor biased to cutoff when its input is less than the second voltage value.

17. The apparatus according to claim 16, wherein the transistor is a field effect transistor (FET).

18. The apparatus according to claim 17, wherein the FET is an enhancement mode FET.

19. The apparatus according to claim 15, wherein the memory circuit is a D flip-flop, wherein the voltage reset monitor output is coupled to a D-input of the D flip-flop, the voltage detector output is coupled to a clear input of the D flip-flop, and a Q-output of the D flip-flop is coupled to the inhibit-input of the power supply.

20. The apparatus according to claim 15, wherein the continuous power source is a battery.

21. The information handling system according to claim 1, wherein the first voltage value is about 95 percent of the at least one voltage normal operating value.

22. The information handling system according to claim 1, wherein the second voltage value is about 0.7 volts.

23. The method according to claim 10, wherein the first voltage value is about 95 percent of the at least one voltage normal operating value.

24. The method according to claim 10, wherein the second voltage value is about 0.7 volts.

25. The apparatus according to claim 15, wherein the first voltage value is about 95 percent of the at least one voltage normal operating value.

26. The apparatus according to claim 15, wherein the second voltage value is about 0.7 volts.

27. An information handling system having power supply shutdown control, said system comprising:

an information handling system having a power supply, the power supply adapted for receiving power from an external power source and providing a plurality of voltages necessary to power the information handling system, the power supply having an on-input and an inhibit-input, wherein the on-input is used to turn the power supply on and off and the inhibit-input is used to prevent the power supply from being turned on; and

a shutdown control circuit for monitoring the plurality of voltages from the power supply, the shutdown control circuit having an output coupled to the inhibit-input of the power supply, wherein when any one of the plurality of voltages is less than a respective nominal operating voltage and greater than a minimum voltage the shutdown control circuit output sends a disable signal to the inhibit-input to prevent the power supply from being turned on, and when all of the plurality of voltages are less than or equal to the minimum voltage or greater than or equal to the respective nominal operating voltages the shutdown control circuit output sends an enable signal to the inhibit-input to allow the power supply to be turned on.

28. The information handling system according to claim 27, wherein the shutdown control circuit comprises:

a plurality of voltage reset monitors each having an output and an input coupled to a respective one of the plurality of voltages from the power supply, wherein each output of the plurality of voltage reset monitors is at a first logic level when a respective one of

the plurality of voltages is greater than or equal to the respective nominal operating voltage and at a second logic level when the respective one of the plurality of voltages is less than the respective nominal operating voltage and greater than the minimum voltage;

a plurality of voltage detectors, each of the plurality of voltage detectors having an input coupled to the respective one of the plurality of voltages from the power supply and an output, wherein the voltage detector output is at the first logic level when the respective one of the plurality of voltages from the power supply is greater than or equal to the minimum voltage and is at the second logic level when the respective one of the plurality of voltages is less than the minimum voltage;

a plurality of memory circuits, each of the plurality of memory circuits having an input coupled to the output of the respective voltage reset monitor, a clear input coupled to output of the respective voltage detector, and an output coupled to an input of a logic OR circuit, wherein the logic OR circuit has a output coupled to the inhibit-input of the power supply; and

a continuous power source that supplies power to the plurality of voltage detectors and the plurality of memory circuits; wherein whenever a one of the plurality of voltage reset monitor outputs goes from the first logic level to the second logic level the respective output of the one of the plurality of memory circuits is set to the first logic level and when the voltage detector output is at the second logic level the respective output of the one of the plurality of memory circuits is reset to the second logic level, whereby if any one or more outputs of the plurality of memory circuits is at the first logic level then the OR circuit output sends the disable signal to the inhibit-input to prevent the power supply from being turned on, and when all of the outputs of the plurality of

memory circuits are at the second logic level the OR circuit output sends the enable signal to the inhibit-input to allow the power supply to be turned on.

29. A method for preventing a power supply from being re-energized before all of a plurality of operating voltages therefrom are below a minimum voltage level, said method comprising the steps of:

providing a power supply in an information handling system that receives power from an external power source and provides a plurality of voltages necessary to power the information handling system, the power supply having an on-input and an inhibit-input, wherein the on-input turns the power supply on and off and the inhibit-input prevents the power supply from being turned on; and

monitoring each of the plurality of voltages from and controlling the power supply with a shutdown control circuit, the shutdown control circuit having an output coupled to the inhibit-input of the power supply, wherein when any one of the plurality of voltages is less than a respective nominal operating voltage and greater than a minimum voltage the shutdown control circuit output sends a disable signal to the inhibit-input to prevent the power supply from being turned on, and when all of the plurality of voltages are less than or equal to the minimum voltage or greater than or equal to the respective nominal operating voltages the shutdown control circuit output sends an enable signal to the inhibit-input to allow the power supply to be turned on.

30. The method according to claim 29, wherein the steps of monitoring each of the plurality of voltages from and controlling the power supply, comprise the steps of:

monitoring each of the plurality of voltages from the power supply with a voltage reset monitor, wherein the voltage reset monitor is at a first logic level when the

respective one of the plurality of voltages is greater than or equal to the respective nominal operating voltage and at a second logic level when the respective one of the plurality of voltages is less than the respective nominal operating voltage and greater than the minimum voltage;

monitoring each of the plurality of voltages from the power supply with a voltage detector, wherein the voltage detector is at the first logic level when the respective one of the plurality of voltages from the power supply is greater than or equal to the minimum voltage and is at the second logic level when the respective one of the plurality of voltages is less than the minimum voltage;

storing each of the voltage reset monitor logic levels in a respective memory circuit; and

resetting the respective memory circuit to the first logic level when the respective one of the plurality of voltages from the power supply is less than the minimum voltage; and

logically combining the memory circuit logic levels such that whenever any memory circuit logic level is at the second logic level the shutdown control circuit output sends a disable signal to the inhibit-input to prevent the power supply from being turned on.